

301402**October, 2020**

B.Tech. (CE/IT/CSE) - IV SEMESTER
Computer Organization and Architecture
(PCC-CS-402)

Time : 3 Hours]

[Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part -A in short.*
2. *Answer any four questions from Part -B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*



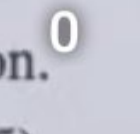
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PART - A

1. (a) Define Memory address register. (1.5)
- (b) What do you understand by Bus arbitration. (1.5)
- (c) Perform $(12)_{10} - (14)_{10}$ using 2's complement notation. (1.5)
- (d) What is the difference between a subroutine and an Interrupt Service Routine (ISR)? (1.5)



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(e) Under what situations the micro program counter is not incremented after a new instruction is fetched from micro program memory? (1.5)

(f) Determine the four pages that are resident in the main memory after each page reference change if the replacement algorithm used is FIFO if the following references to pages are made

4 2 0 1 2 6 1 4 0 1 0 2 3 5 7 (1.5)

(g) Differentiate between SRAM and DRAM. (1.5)

(h) How many memory chips are needed to construct a $2M \times 16$ memory system using $512k \times 8$ memory chips? (1.5)

(i) What are the major characteristics of a Pipeline? (1.5)

(j) Draw a space time diagram for 4-segment pipeline showing the time to process six tasks. (1.5)

PART - B

2. (a) What are addressing modes? An instruction is stored at location 800 with address field at location 801. The address field has the value 900. A process or register Rx contains the number 800. Evaluate the effective address if the addressing mode of instruction is (i) direct (ii) immediate (iii) relative (iv) register indirect

(b) What are different types of instruction in a basic CPU? Name few of each type.

(c) Design a 4-bit carry look-ahead adder. (4)

(d) What is RTL? Write RTL representation and interpretation for a loading a register. (3)

3. (a) Represent 52.21875 in 32-bit binary floating point format. (3)

(b) Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied. Assume 4-bit registers that hold signed numbers:

(i) $(+5) \times (+3)$

(ii) $(-5) \times (-3)$. (2)

(c) Show the contents of registers E, A, Q and SC during the process of division of 21

(i) 10110011 by 1001

(ii) 11110000 by 0011.

(use a dividend of 8bits). (5)

(d) Starting from an initial value of $R=11110110$, determine the sequence of binary values of R after a logical shift-left, followed by a circular shift-right, followed by a logical shift-right and a circular shift-left (5)

4. (a) What is meant by Micro programmed Control? Draw and explain design of such a control unit. (10)

(b) What are static and dynamic memories? Explain. (5)

5. (a) With the help of a diagram, describe USB architecture. (5)

(b) Explain DMA. Discuss DMA controller using suitable block diagrams. (5)

(c) Explain program controlled an interrupt initiated data transfer. (5)

6. (a) Draw and explain the flowchart for interrupt cycle. (5)

(b) Explain set associative cache organization with a suitable example. (5)

(c) Explain the different write policies.

(d) What is meant by memory interleaving? Explain. (3)



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7. Write short notes on :

(a) Pipelining and its hazards.

(b) Booth's multiplication.



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